AMENDMENTS TO THE CLAIMS

Please amend claims 3-5, 28, 40, 46, 48, 49, and 54 as follows.

Please cancel claim 56.

Please add new claims 57 and 58.

The following listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended): A synchronous memory circuit comprising:
an address bus for receiving an address;
at least two memory blocks each of which is capable to be accessed at said address; and
a data bus for receiving data items for transfer to or from the memory blocks,
wherein in two consecutive clock cycles at least a first and a second write data items corresponding to a first write burst operation are capable of being transferred sequentially to the memory circuit via the data bus and at least a first and second read data items corresponding to a first read burst operation are capable of being provided sequentially by the memory circuit via the data bus, and
wherein the data bus is capable of receiving data corresponding to the write burst operation and providing data corresponding to the read burst operation with no dead cycles therebetween.

2. (Previously presented): The memory circuit of claim 1 wherein the at least first and second write data items are provided on the data bus at least one clock cycle after the first write burst operation is initiated, and the at least first and second read data items are provided on the data bus at least one clock cycle after the first read burst operation is initiated.

3. (Currently amended): The memory circuit of claim 2 further comprising at least one input terminal for receiving at least one read/write control signal for indicating a read burst or a write burst operation, wherein each of the first write burst operation and the first read burst operation is initiated upon an edge of a clock cycle by asserting the read/write control signal

to indicate ~~a~~ the write burst or ~~a~~ the read burst operation and providing a burst address at the address bus both prior to the rising edge of the clock cycle.

4. (Currently amended): The memory circuit of claim 1 wherein in two and a half consecutive clock cycles at least a third and a fourth data items corresponding to a second write or read burst operation are capable of being transferred to or from respective at least two memory blocks and at least a fifth and sixth data items corresponding to a third write or read burst operation are capable of being transferred to or from respective the at least two memory blocks.

5. (Currently amended): The memory circuit of claim 4 wherein transferring the at least third and fourth data items to or from the respective at least two memory blocks overlaps with transferring the at least fifth and sixth data items from respective the at least two memory blocks during half a clock cycle.

6. (Previously presented): The memory circuit of claim 1 wherein the first write burst operation comprises writing at least a third and fourth write data items to respective two memory blocks so that writing the third write data item overlaps with writing the fourth write data item, the at least third and fourth write data items corresponding to a last write burst operation prior to the first write burst operation.

7. (Previously presented): The memory circuit of claim 6 wherein each of the at least third and fourth write data items is written in one clock cycle, and writing the third write data item overlaps with writing the fourth write data item during half a clock cycle.

8. (Previously presented): The memory circuit of claim 1 wherein the first read burst operation comprises reading the at least first and second read data items from respective two memory blocks so that reading the first read data item overlaps with reading the second read data item.

9. (Previously presented): The memory circuit of claim 8 wherein each of the at least first and second read data items is read in one clock cycle, and reading the first read data item overlaps with reading the second read data item during half a clock cycle.

10. (Previously presented): The memory circuit of claim 1 further comprising an output circuit for receiving the at least first and second read data items from respective at least two memory blocks in the first read burst operation and allowing the first read data item to be provided on the data bus half a clock cycle after the first read burst operation is initiated, and allowing the second read data item to be provided on the data bus one clock cycle after the first read burst operation is initiated.

11. (Previously presented): The circuit of claim 10 wherein the output circuit is enabled only when a valid read data item is to be provided on the data bus so that no external tracking of the progress of a read burst operation is required.

12. (Previously presented): The memory circuit of claim 11 further comprising at least one input terminal for receiving at least one read/write control signal for initiating a read burst operation or a write burst operation, wherein the output circuit is enabled by a 3-state signal generated from the read/write control signal.

13. (Previously presented): The memory circuit of claim 10 wherein the output circuit comprises a multiplexer for receiving a clock signal and the at least first and second read data items and sequentially transferring to an output bus of the multiplexer the at least first and second read data items in accordance with the state of the clock signal.

14. (Previously presented): The memory circuit of claim 10 further comprising at least two registers for providing both a burst address received at the address bus and at least one read/write control signal received at at least one input terminal of the memory circuit to the at least two memory blocks sequentially in one clock cycle.

15. (Previously presented): The circuit of claim 14 wherein at the initiation of the first read burst operation the at least two registers provide both a read burst address received at the address bus and the least one read/write control signal indicating a read burst operation to one of the at least two memory blocks, and half a clock cycle after the initiation of the first read burst operation the at least two registers provide both the read burst address and the at least one read/write control signal indicating a read burst operation to the other one of the at least two memory blocks.

16. (Previously presented): The circuit of claim 14 wherein the at least two registers are serially connected, and one of the at least two registers receives the clock signal and the other register receives the compliment of the clock signal.

17. (Previously presented): The memory circuit of claim 1 wherein in the first write burst operation at least a third and fourth write data items are written to respective at least two memory blocks, the third and fourth write data items corresponding to a last write burst operation prior to the first write burst operation.

18. (Previously presented): The memory circuit of claim 17 further comprising a multiplexer for selecting for transfer to the at least two memory blocks one of a write burst address stored in a first register and a burst address provided on the address bus, wherein in the first write burst operation the multiplexer selects a first write burst address stored in the first register, the first write burst address corresponding to the last write burst operation, and in the first read burst operation the multiplexer selects a first read burst address provided on the address bus.

19. (Previously presented): The memory circuit of claim 18 wherein the first register holds a write burst address until a next write burst is initiated.

20. (Previously presented): The memory circuit of claim 17 wherein the third write data item is written to one of the at least two memory blocks at the initiation of the first write burst

operation, and the fourth write data item is written to the other one of the at least two memory blocks half a clock cycle after the initiation of the first write burst operation.

21. (Previously presented): The memory circuit of claim 20 further comprising at least two registers for storing respective at least two write data items provided on the data bus in a write burst operation, wherein in the last write burst operation the at least third and fourth write data items are stored in the respective at least two registers, the at least two registers providing the third write data item to one of the at least two memory blocks at the initiation of the first write burst operation and providing the fourth write data item to the other one of the at least two memory blocks half a clock cycle after the initiation of the first write burst operation.

22. (Previously presented): The memory circuit of claim 21 wherein one of the at least two registers receives a clock signal and the other one of the at least two registers receives the complement of the clock signal.

23. (Previously presented): The memory circuit of claim 21 wherein if a read burst address for the first read burst operation and a write burst address for the first write burst operation are the same and the first write burst operation is followed by the first read burst operation, in the first read burst operation the at least first and second write data items stored in respective at least two registers in the first write burst operation are sequentially provided at the data bus.

24. (Previously presented): The memory circuit of claim 22 further comprising a comparator for comparing a burst address of a current burst operation with a write burst address of a preceding write burst operation stored in a third register, wherein in the first read burst operation the comparator compares a read burst address corresponding to the first read burst operation with a write burst address corresponding to the first write burst operation and allows the at least first and second write data items stored in respective two registers in the first write burst operation to be provided at the data bus if the read burst address and the write

burst address are the same and the first write burst operation is followed by the first read burst operation.

25. (Previously presented): The memory circuit of claim 1 wherein the memory circuit is a static random access memory (SRAM).

26. (Previously presented): The memory circuit of claim 1 further comprising a circuit for generating an echo clock signal from the clock signal such that the echo clock signal is active only when a read data item is provided on the data bus.

27. (Previously presented): The memory circuit of claim 1 wherein the data bus comprises:

a data-in bus for receiving write data items; and

a data-out bus for providing read data items.

28. (Currently amended): A method of accessing a synchronous memory circuit, the method comprising ~~the~~:

(A) initiating a first write burst operation for sequentially transferring at least a first and second write data items to the memory circuit in a first clock cycle; and

(B) initiating a first read burst operation for sequentially transferring at least a first and second read data items from the memory circuit in a second clock cycle,

wherein the first and second clock cycles are two consecutive clock cycles.

29. (Previously presented): The method of claim 28 further comprising:

(C) initiating the first write burst operation in a third clock cycle, the first clock cycle being the next sequential clock cycle after the third clock cycle; and

(D) initiating the first read burst operation in a fourth clock cycle, the second clock cycle being the next sequential clock cycle after the fourth clock cycle.

30. (Previously presented): The method of claim 29 wherein:

act (C) comprises:

(E) asserting a read/write control signal on an input terminal of the memory circuit to indicate a write burst operation prior to a rising edge of the third clock cycle; and

(F) providing a first write burst address on an address bus of the memory circuit prior to the rising edge of the third clock cycle, and

act (D) comprises:

(G) asserting the read/write control signal to indicate a read burst operation prior to a rising edge of the fourth clock cycle; and

(H) providing a first read burst address on the address bus prior to the rising edge of the fourth clock cycle.

31. (Previously presented): The method of claim 28 wherein the memory circuit includes at least two memory blocks, the method further comprising:

(I) transferring at least a third and fourth data items corresponding to a second burst operation to or from respective at least two memory blocks; and

(J) transferring at least a fifth and sixth data items corresponding to a third burst operation to or from respective at least two memory blocks,

wherein acts (I) and (J) are carried out in two and half consecutive clock cycles.

32. (Previously presented): The method of claim 31 wherein said transferring the at least third and fourth data items to or from respective at least two memory blocks overlaps with said transferring the at least fifth and sixth data items to or from respective at least two memory blocks during half a clock cycle.

33. (Previously presented): The method of claim 28 wherein the memory circuit includes two memory blocks and act (A) comprises:

(K) writing at least a third and fourth write data items to respective two memory blocks so that writing the third write data item overlaps with writing the fourth write data item, the at least third and fourth write data items corresponding to a last write burst operation prior to the first write burst operation

34 (Previously presented): The method of claim 33 wherein act (K) comprises:

(L) writing the third write data item in one clock cycle; and

(M) writing the fourth write data item in one clock cycle,

wherein said writing the third write data item overlaps with said writing the fourth write data item during half a clock cycle.

35. (Previously presented): The method of claim 28 wherein the memory circuit includes two memory blocks and act (B) comprises:

(N) reading the at least first and second read data items from respective two memory blocks so that reading the first read data item overlaps with reading the second read data item.

36. (Previously presented): The method of claim 35 wherein act (N) comprises:

(O) reading the first read data item in one clock cycle; and

(P) reading the second read data item in one clock cycle,

wherein said reading the first read data item overlaps with said reading the second read data item during half a clock cycle.

37. (Previously presented): The method of claim 28 further comprising:

(Q) generating an echo clock signal from a clock signal, the echo clock signal being active only when a read data item is read from the memory circuit.

38. (Previously presented): A synchronous memory circuit comprising:

an address bus for receiving a burst address;

two memory blocks;

data bus for transferring data corresponding to the burst address to or from the two memory blocks;

a control input terminal for receiving a read/write control signal for indicating a read burst or a write burst operation, wherein a burst operation is initiated upon a rising edge of a clock cycle by asserting the read/write control signal to indicate a write burst or a read burst operation and providing an address at the address bus both prior to the rising edge of the clock cycle;

an output circuit for receiving two read data items from respective two memory blocks in a first read burst operation and allowing one of the two read data items to be provided on the data bus half a clock cycle after the first read burst operation is initiated, and allowing the other one of the two read data items to be provided on the data bus one clock cycle after the first read burst operation is initiated; and

a first and second registers for storing respective two write data items provided on the data bus in a first write burst operation, wherein one of the two write data items is written to one of the two memory blocks at the initiation of a next write burst operation following the first write burst operation, and the other one of the two write data items is written to the other one of the two memory blocks half a clock cycle after the initiation of the next write burst operation,

wherein in two consecutive clock cycles the two write data items are capable of being transferred to the memory circuit via the data bus and the two read data items are capable of being transferred from the memory circuit via the data bus.

39. (Previously presented): The memory circuit of claim 38 further comprising:

a multiplexer for selecting for transfer to the two memory blocks one of a write burst address stored in a third register and a burst address provided on the address bus, wherein in the next write burst operation the multiplexer selects a first write burst address stored in the third register, the first write burst address corresponding to the first write burst operation, and in the first read burst operation the multiplexer selects a first read burst address provided on the address bus; and

a fourth and fifth serially connected registers for providing both the read/write control signal and the burst address selected by the multiplexer to one of the two memory blocks at the initiation of a burst operation and to the other one of the two memory blocks half a clock cycle after the initiation of the burst operation.

40. (Currently amended): The memory circuit of claim 39 wherein each of the first, third, and fourth registers receives the clock signal, and each of the second and fifth registers ~~recieves~~ receives the complement of the clock signal.

41. (Previously presented): The memory circuit of claim 38 further comprising a comparator for comparing a burst address at the address bus with a write burst address stored in a third register, wherein in a second read burst operation corresponding to a second read burst address if the second read burst address is the same as a second write burst address stored in the third register the comparator causes a first and second write data items stored in the respective first and second registers to be provided at the data bus, the first and second write data items and the second write burst address corresponding to a last write burst operation before the second read burst operation.

42. (Previously presented): The memory circuit of claim 41 wherein the output circuit comprises a multiplexer having four input buses for receiving a respective four read data items two read data items from the respective two memory blocks and two read data items from the respective two first and second registers, and two control input terminals for receiving a respective clock signal and signal generated from the comparator, wherein the multiplexer selects one of the four read data items for transfer to the data bus in accordance with the states of the clock signal and the signal generated from the comparator.

43. (Previously presented): The memory circuit of claim 38 wherein the output circuit comprises:

a multiplexer for sequentially transferring to an output bus of the multiplexer the two read data items in accordance with the state of the clock signal; and

an output buffer for receiving the two read data items from the output bus of the multiplexer and providing the two read data items to the data bus when enabled, wherein the output buffer is enabled only when a valid read data item is to be provided on the data bus so that no external tracking of the progress of a read burst operation is required.

44. (Previously presented): The memory circuit of claim 38 wherein each of the two memory blocks comprises an address bus for receiving a burst address, an input terminal for receiving a read/write control signal for indicating a read burst or a write burst operation, a data-in bus for receiving a write data item, and a data-out bus for providing a read data item, wherein each of the two memory blocks operates asynchronously.

45. (Previously presented): The memory circuit of claim 38 wherein the memory circuit is a static random access memory (SRAM).

46. (Currently amended): A synchronous memory circuit comprising:
a first memory block and a second memory block;
a data bus for transferring data to or from the first memory block and the second memory block; and
an output circuit for receiving a first read data item from the first memory block and receiving a second read data item from the second memory block in a first read operation, wherein each of the first and second read data items initiated by the first read operation is read in one clock cycle, and reading the first read data item overlaps with reading the second read data item ~~and allowing the first read data item to be provided on the data bus within one clock cycle after the first read operation is initiated~~.

47. (Previously presented): The circuit of claim 46 wherein the output circuit comprises a transmission gate for selecting for transfer to the data bus the first read data item in accordance with the state of a clock signal.

48. (Currently amended): The memory circuit of claim 47 further comprising:
an address bus for receiving an address; and
a control input terminal for receiving a read/write control signal for indicating a read or a write operation,
wherein the first read operation is initiated upon a rising edge of a clock cycle by asserting the read/write control signal to indicate a read operation and providing a first address at the address bus both prior to the rising edge of the clock cycle, the first read data item corresponding to the first address.

49. (Currently amended): The memory circuit of claim 46 wherein ~~the memory circuit further comprises a second memory block, the output circuit receiving a second read data item from the second memory block in the first read operation and allowing~~ the output circuit

allows the first read data item to be provided on the data bus within one clock cycle after the first read operation is initiated and allows the second read data item to be provided on the data bus after one clock cycle after the first read operation is initiated.

50. (Previously presented): The memory circuit of claim 49 wherein the first read operation is a first read burst operation.

51. (Previously presented): The circuit of claim 50 wherein the control circuit comprises a multiplexer for sequentially selecting for transfer to the data bus the first and second read data items in accordance with the state of a clock signal.

52. (Previously presented): The memory circuit of claim 51 further comprising:
an address bus for receiving a burst address; and
a control input terminal for receiving a read/write control signal for indicating a read burst or a write burst operation,
wherein the first read burst operation is initiated upon a rising edge of a clock cycle by asserting the read/write control signal to indicate a read burst operation and providing a first burst address at the address bus both prior to the rising edge of the clock cycle, the first and second data items representing a burst of two data items corresponding to the first burst address.

53. (Previously presented): The circuit of claim 46 wherein the memory circuit is a static random access memory (SRAM), or a dynamic random access memory (DRAM), or a programmable read only memory (PROM).

54. (Currently amended): A memory circuit comprising:
a clock terminal for receiving a clock signal;
an address bus for receiving an address;
a data bus for receiving write data and providing read data; and

wherein the memory circuit is capable to perform a write burst operation in which the memory circuit receives one read address from the address bus and the memory circuit also receives, sequentially, two write data items from the data bus;

wherein the memory circuit is capable to perform a read burst operation in which the memory circuit receives one write address on the address bus and the memory circuit provides, sequentially, two ~~write~~ read data items on the data bus;

wherein the memory circuit is capable to receive a new read or write address in each clock cycle of the clock signal, so that consecutive read and write burst operations are capable to be performed sequentially in any order with the respective read and write addresses being received by the memory circuit in consecutive clock cycles, without any dead clock cycles there between.

55. (Previously presented): The memory circuit of claim 54 wherein receiving an address in one burst operation is capable to overlap with receiving or providing data in a previous burst operation.

56. (Canceled)

57. (New): The memory circuit of claim 1 wherein the first write burst operation occurs before the first read burst operation.

58. (New): The memory circuit of claim 1 wherein the first read burst operation occurs before the first write burst operation.